

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims

1-5 (Cancelled)

6. (Currently Amended) A semiconductor device, comprising:

a carrier substrate having a bond pad;

a first microelectronic die ~~substrate, the first microelectronic die substrate~~  
~~including, including:~~

an active side and a ~~back side~~backside,

an active side interconnect, ~~the active side interconnect~~ disposed on the  
active side, and coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the ~~back side~~backside, coupled to  
and in substantial vertical alignment with the active side interconnect,  
a redistributed interconnect of the backside interconnect, disposed on the  
backside, coupled to and offset from the backside interconnect;

an interconnect material comprising a conductive material without a wire stem,  
the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die ~~substrate~~ electrically and directly  
coupled to the interconnect material.

7. (Currently Amended) The semiconductor device of claim 6, wherein the first ~~substrate-microelectronic die~~ comprises:
- a metal layer having a first side and a second side;
  - a first dielectric layer adjacent to the first side of the metal layer;
  - a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;
  - a second dielectric layer adjacent to the second side of the metal layer; and
  - a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.
8. (Currently Amended) The semiconductor device of ~~Claim-claim~~ 6, wherein the redistributed interconnect comprises:
- a conductive trace coupled to and extending from the backside interconnect to a selected location;
  - a third dielectric layer overlaying the conductive trace; and
  - an aperture in the third dielectric layer at the selected location.
9. (Currently Amended) The semiconductor device of Claim 8, wherein the selected location for the redistributed interconnect corresponds to the interconnect of the second microelectronic die ~~substrate~~.
10. (Cancelled)
11. (Currently Amended) The semiconductor device of claim 6, wherein the second microelectronic die ~~substrate~~ is coupled to the redistributed interconnect by a process selected from the group consisting of reflow bonding, thermal compression bonding, and ultrasonic bonding.

12. (Currently Amended) The semiconductor device of ~~Claim-claim~~ 6, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.

13. (Withdrawn) A method comprising:  
providing an active side interconnect to an active side of a substrate;  
providing a backside interconnect to a back side of the substrate with the backside interconnect being coupled to and in substantial vertical alignment with the active side interconnect; and  
providing a redistributed interconnect of the backside interconnect on the backside, the redistributed interconnect being coupled to and offset from the backside interconnect.

14. (Withdrawn) The method of Claim 13, wherein providing the redistributed interconnect comprises:  
depositing a conductive trace on the back side;  
coupling the conductive trace to the backside interconnect;  
extending the conductive trace to a selected location;  
placing a third dielectric layer over the conductive trace; and  
forming an aperture in the third dielectric layer at the selected location.

15. (Withdrawn) The method of Claim 13, wherein providing the backside interconnect comprises forming a via that extends from the backside interconnect through a second dielectric layer to a metal layer and filling the via with an electrically conductive material.

16. (Withdrawn) The method of claim 13, further comprising;  
providing a carrier substrate having a bond pad  
providing a second substrate having an interconnect;  
coupling the active side interconnect to the carrier substrate bond pad; and  
coupling the interconnect of the second substrate to the redistributed  
interconnect.
17. (Withdrawn) The method of Claim 16, wherein coupling the interconnect of the  
second substrate to the redistributed interconnect is performed by a process selected  
from the group including reflow bonding, thermal compression bonding or ultrasonic  
bonding.
18. (Withdrawn) A method for redistributing interconnects, comprising:  
providing a substrate having an active side and a backside, the active side  
having an active side interconnect;  
forming a via in the backside extending from a surface of the backside to a metal  
layer within the substrate;  
filling the via with an electrically conductive material such that a backside  
interconnect is formed at or substantially near the surface of the backside and in  
electrical communication with the metal layer;  
depositing a conductive trace on the backside surface such that the conductive  
trace extends from the backside interconnect to a selected location on the back side  
surface;  
depositing a dielectric layer on the back side surface such that it overlays the  
conductive trace; and  
defining a redistributed interconnect of the backside interconnect at the selected  
location.

19. (Withdrawn) The method of Claim 18, wherein defining the redistributed interconnect comprises forming an aperture in the dielectric layer at the selected location to expose a portion of the conductive trace.
20. (Withdrawn) The method of Claim 19, wherein forming the aperture comprises etching a portion of the dielectric layer at the selected location to expose a portion of the conductive trace.
21. (Withdrawn) The method of Claim 18, further comprising choosing the selected location to correspond to a location of a complementary interconnect of a substrate in facing relationship there with.
22. (Withdrawn) The method of Claim 18, wherein depositing the conductive trace comprises forming a patterned electrically conductive layer on the backside surface using a photolithography process.
23. (Withdrawn) The method of Claim 18, further comprising depositing a conductive interconnect material into the dielectric aperture such that the conductive interconnect material is coupled to the redistributed interconnect and extends above the dielectric layer.
24. (Withdrawn) The method of claim 18, further comprising;  
providing a carrier substrate having a bond pad;  
providing a second substrate having an interconnect;  
coupling the active side interconnect to the carrier substrate bond pad; and  
coupling the interconnect of the second substrate to the redistributed interconnect.

25. (Withdrawn) The method of Claim 24, wherein coupling the interconnect of the second substrate to the redistributed interconnect is performed by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.

26. (Currently Amended) A semiconductor device, comprising:

a carrier substrate having a bond pad;

~~a first microelectronic die-substrate; the first microelectronic die-substrate including;~~  
including;

an active side and a ~~back-side~~backside,

an active side interconnect;~~the active side interconnect~~ disposed on the active side;and coupled to the bond pad of the carrier substrate,

a backside interconnect disposed on the ~~back-side~~backside, coupled to

and in substantial vertical alignment with the active side interconnect,

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect;

an interconnect material consisting an electrically conductive reflowable material, the interconnect material being coupled directly with the redistributed interconnect; and

an interconnect of a second microelectronic die ~~substrate~~ electrically and directly coupled to the interconnect material.

27. (Previously Presented) The semiconductor device of claim 26, wherein said electrically conductive reflowable material is lead solder or lead-free solder.

28. (Currently Amended) A semiconductor device, comprising:  
a carrier substrate having a bond pad;  
a first microelectronic die ~~substrate~~, the first microelectronic die ~~substrate~~  
including,  
an active side and a ~~back-side~~backside,  
an active side interconnect, ~~the active side interconnect~~ disposed on the  
active side, ~~and~~ coupled to the bond pad of the carrier substrate,  
a backside interconnect disposed on the ~~back-side~~backside, coupled to  
and in substantial vertical alignment with the active side interconnect,  
a redistributed interconnect of the backside interconnect, disposed on the  
backside, coupled to and offset from the backside interconnect;  
an interconnect material consisting an electrically conductive adhesive, the  
interconnect material being coupled directly with the redistributed interconnect; and  
an interconnect of a second microelectronic die ~~substrate~~ electrically and directly  
coupled to the interconnect material.
29. (Previously Presented) The semiconductor device of claim 27, wherein said  
interconnect material is silver-loaded epoxy.
30. (New) The semiconductor device of claim 6, wherein the second microelectronic  
die comprises an active side and a backside, and wherein the interconnect is disposed  
on the active side of the second microelectronic die.

31. (New) The semiconductor device of claim 6, wherein the second microelectronic die comprises:

a first side and a second side, the interconnect being disposed on a selected one of the first side and the second side, and another interconnect being disposed on the non-selected one of the first side and the second side, and

a via extending from the first side to the second side to electrically couple the interconnect to the other interconnect.

32. (New) The semiconductor device of claim 31, wherein the second microelectronic die further includes a redistributed interconnect of a selected one of the interconnects of the second microelectronic die, wherein the redistributed interconnect is coupled to and offset from the selected interconnect.